



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,270	01/24/2002	Janusz M. Kucharski	100.323US01	8559
34206	7590	03/10/2004	EXAMINER	
FOGG AND ASSOCIATES, LLC P.O. BOX 581339 MINNEAPOLIS, MN 55458-1339			DINH, TUAN T	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/056,270

Applicant(s)

KUCHARSKI, JANUSZ M.

Examiner

Tuan T Dinh

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 8-10, 14, 15, 19-21, 25 and 26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 11-13, 16-18, 22-24 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwane (U. S. Patent 5,719,750).

As to claim 1, Iwane discloses an electronic device (column 4, line 12) as shown in figures 2-13 comprising:

a circuit board (10, column 3, line 42);

a first circuit (6a-6c) disposed on a first side of the circuit board, the first circuit connected to a first ground plane (3a, column 3, lines 58-59) of the circuit board (10);

a second circuit (6d-6e) disposed on a second side of the circuit board, wherein the second side is opposite the first side, the second circuit connected to a second ground plane (3b, column 3, lines 58-59) of the circuit board; and

wherein the first and second ground planes respectively lie in different planes (see figures 2, 6, 8, and 10) of the circuit board (10) and are electrically interconnected by a conductive trace (1, 2, and 4) disposed within the circuit board.

As to claims 11 and 13, Iwane discloses the device as shown in figures 2, 6, 8, and 10 wherein the circuit board (10) comprises two or more layers (5a-5e, column 3, lines 43-44) disposed between the first and second sides.

As to claim 12, Iwane discloses the device as shown in figures 2-10 wherein the first ground plane (3a) is disposed on one of the two or more layers (5c-5e) and the second ground plane (3b) is disposed on another of the two or more layers (5a-5d).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2-7, 16-18, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwane ('750) in view of Hirashiro et al. (JP 406069680A, hereafter JP).

As to claims 2-4, Iwane discloses all of the limitations of claimed invention, except for the first circuit having a switch mode power supply, which is a forward-type switch mode power supply or a flyback-type switch mode power supply.

JP shows an inverter module as shown in figures 1-3 comprising a printed circuit board (3) having a power circuit (5a), the power circuit (5a) comprises a capacitor (18) and an inductor (26) capable of being either forward/flyback type switch mode power supplies.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a first circuit having a switch mode power supply (forward/flyback type switch mode power supply), as taught by JP, employed in the

Art Unit: 2827

printed circuit board of Iwane in order to provide a switching circuit and operate a power for a circuit board.

As to claims 5-6, JP shows a second circuit controls a first circuit, and the first circuit is adapted to power the second circuit.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a second circuit controls a first circuit, and the first circuit is adapted to power the second circuit, as taught by JP, employed in the printed circuit board of Iwane in order to provide control and power facilitate circuit for a circuit board.

As to claims 7, 18, Iwane and JP do not show the second circuit operates at current levels substantially lower than the first circuit.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a second circuit operates at current levels substantially lower than a first circuit in order to control a power that applied on the PCB as taught by Iwane and JP.

As to claims 16-17, Iwane discloses all of the limitations of the claimed invention, except for a power loop and a control circuit disposed on first and second surfaces of the PCB, and the power loop is adapted to power the control circuit.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a power loop and a control circuit disposed on first and second surfaces of the PCB, as taught by JP, employ in the PCB of Iwane for purpose of providing power and control input/output signals for the PCB.

Art Unit: 2827

As to claims 22 and 24, Iwane discloses the device as shown in figures 2, 6, 8, and 10 wherein the circuit board (10) comprises two or more layers (5a-5e, column 3, lines 43-44) disposed between the first and second sides.

As to claim 23, Iwane discloses the device as shown in figures 2-10 wherein the first ground plane (3a) is disposed on one of the two or more layers (5c-5e) and the second ground plane (3b) is disposed on another of the two or more layers (5a-5d).

Response to Arguments

5. Applicant's arguments filed 12/15/03 have been fully considered but they are not persuasive.

Applicant argues:

(a) Iwane does not disclose components 6a-6e, respectively as first and second circuits.

(b) the combination of Iwane in view of Hirasgiro (JP) fails to apply 103 rejection on claims 2-7, 16-18, and 22-24.

Examiner disagrees.

Response to arguments (a) and (b), Iwane discloses the components (6a-6e) being represent to be of a frequency synthesizer (108), a transmitter RF pre-amplifier (110), and a transmitter RF power amplifier (109), see column 8, lines 21-25, respectively. Those components include circuits for input/output signals generated inside the components. Therefore, it is believed that the 102(b) rejection as sets forth claim 1 is proper.

With respect to claims 2-4, Iwane discloses the components (6a-6e) as explained above disposed on the circuit board, and Hirashiro (JP'680A) teaches a power circuit (5a) mounted on a circuit board (3), the power circuit (5a), which is a circuit to provide a power for the circuit board, does not limiting in what applicable being used, and it could be an amplifier, a switching circuit, a control circuit, or a power loop circuit. Therefore, it would have been obvious having ordinary skill in the art that to employ the component of Hirashiro (JP) in the electronic device of Iwane for the purpose of providing switching and power operation circuit to the circuit board. Therefore, it is believed that the 103(a) rejection of the combination of Iwane in view of Hirashiro (JP) as set forth claims 2-4 is proper.

In additional, Hirashiro (JP) reference, with respect to claims 5-6, shows the power circuit (5a) having various functions as explained insofar, the power circuit (5a) can be control or adapt to power to the components mounted on the circuit board.

Therefore, it is believed that the 103(a) rejection of the combination of Iwane in view of Hirashiro (JP) as set forth claims 5-6 is proper.

With respect to claim 7, because JP reference teaches the power circuit on the circuit board, so that the power circuit can be a power supply to adjust voltage applied on the circuit board. Being adjusting voltage, the power circuit of JP reference is capable of being operated at current levels substantially lower than another component mounted on the circuit board. Thus, claim 7 is proper rejected under 103.

As explained insofar as above. It is believed the rejection under 103 of claims 16-18, and 22-24 are correct.

Art Unit: 2827


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
March 5, 2004.


KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800